REMARKS/ARGUMENTS

1. Amendments to the specification:

The title of the invention has been amended to be descriptive as per examiner's request. Consideration of the amendment to the title is respectfully requested.

Paragraph [0027] of the specification has also been amended to correct a typographical error. No new matter is entered. Consideration of the amended specification is respectfully requested.

2. Amendments to the claims

Claims 1-12 have been cancelled.

Claims 13-22 are newly entered. New claim 13 recites that the method for generating a linked list forms a linked list for a memory in which each entry of the linked list corresponds to a portion of the memory, performs a BIST on the memory to identify a first defective portion of the memory, and then updates the linked list to remove from the linked list the entry of the linked list corresponding to the identified first defective portion of the memory. These limitations are fully supported by paragraphs [0020] through [0024]. No new matter is added. Consideration of claim 13 is respectfully requested.

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New claim 14 recites that the memory being tested by the BIST is used for storing the linked list, and the step of updating the linked list excludes the use of the defective portion of the memory in storing the linked list. These limitations are described in paragraphs [0021] and [0022]. No new matter is added. Consideration of claim 14 is respectfully requested.

New claim 15 recites that the memory being tested by the BIST is a packet buffer for data storage. This is supported by the paragraph [0023] and no new matter is added. Consideration of claim 15 is respectfully requested.

New claim 16 recites that the step of updating the linked list is performed before the BIST is completely through with the entirety of the memory. As described in the paragraph [0022] lines 2-6 and paragraph [0024] lines 2-7, when a defective portion is found by the BIST, the BIST is paused so as to update the linked list. After the linked list is updated according to the found defective portion, the BIST continues to determine the next defective portion. In other words, the linked list is updated before the BIST is completely through with the entirety of the memory. Thus, no new matter is added. Consideration of claim 16 is respectfully requested.

New claim 17 recites that the method of the present invention continues the BIST step to identify a second defective portion and then

updates the linked list accordingly. These limitations are also supported by paragraphs [0021] through [0024]. Obviously, no new matter is added. Consideration of claim 17 is respectfully requested.

New claim 18 recites that the electronic device is a network switch. This is supported by paragraph [0018]. No new matter is added. Consideration of claim 18 is respectfully requested.

New claim 19 recites that the method for generating a linked list forms a linked list for the memory in which the linked list comprises a plurality of entries each having a first pointer field and a second pointer field, the first pointer field for storing a pointer to a corresponding portion of the memory and the second pointer field for storing a pointer to another entry of the linked list; performs BIST on the memory to identify at least one defective portion of the memory; and updates the linked list to remove from the linked list the entry of the linked list corresponding to the identified defective portion of the memory, so that none of the entries of the updated linked list comprises a pointer in the second pointer field that points to the entry corresponding to the identified defective portion. These limitations are fully supported by paragraph [0005] and paragraphs [0020] through [0027]. Therefore, no new matter is added in the new claim 19. Consideration of claim 19 is respectfully requested.

New claims 20 and 21 are the same as the new claims 18 and 15,

respectively. Consideration of claims 20-21 is respectfully requested.

New claim 22 recites similar claim limitations as those shown in new claims 17 and 19, and is also fully supported by paragraph [0005] and paragraphs [0020] through [0027]. No new matter is added therein. Consideration of claim 22 is respectfully requested.

3. Rejection of claims 1-12 under 35 U.S.C 102(e) or 102(a):

Claims 1-12 are rejected under 35 U.S.C 102(e) as being anticipated by Kim et al. (Kim) US Patent No. 6,781,898 or rejected under 35 U.S.C. 102(a) as being anticipated by Chin US Patent Pub. No. 2003/0145250 for reasons of record.

Response:

Claims 1-12 have been cancelled, and are therefore no longer in need of consideration.

4. Patentability of new claims 13-22

Claim 13

In the present invention, a temporary linked list is formed in Step 100

(paragraph [0026], lines 2-4), and then a BIST is performed on the header table 20 for storing the linked list in Step 110 to determine which sections of the header table 20 are defective. The operations of Step 120 are described in paragraph [0022], lines 2-6, "each time a defective section is found in the header table 20, the switch 10 will **pause the BIST**, update the linked list dynamically so as not to use the defective section in the list, and **then continue the BIST**." Additionally, the descriptions of Step 140 in paragraph [0024], lines 2-7 state, "each time a defective page is found in the packet buffer 30, the switch 10 will **pause the BIST**, update the linked list dynamically so as not to use the section corresponding to the defective page of the packet buffer 30, and **then continue the BIST**." According to the above descriptions, it can be appreciated that the **"BIST operation"** and the **"linked list updating operation"** are alternately performed in the exemplary embodiment of the present invention until all sections of the header table and/or all pages of the packet buffer are tested. In other words, the present invention forms a temporary linked list first and then dynamically updates the linked list while performing the BIST operations on the memories.

Kim generates the linked list with a different approach, however. Specifically, Kim performs Defect-Marking-Memory Test process and Defect Row Marking process first, and then performs Defect Row Skipping process to generate the linked list (col. 5 line 65 to col. 6 line 44, and FIG.3). In the Defect-Marking-Memory Test process, the defective rows of the Defect Marking Memory are detected and the addresses of the defective rows are recorded in Defect Address Registers (see col. 6 lines 2-10). In the Defect Row Marking process, the BIST is performed on all memories

other than the Defect Marking Memory. When faults of the memories are detected, a Defect Marking Logic is used to write **marking codes** to the Defect Marking Memory at the defective addresses (see col. 6 lines 17-32). Moreover, as described in col. 6 lines 32-34, "once all addresses are tested, 234, the process shifts to a Defect Row Skipping process." This clearly illustrates that the Defect Row Skipping process for generating the linked list is performed **after** all addresses are tested by BIST according to Kim's disclosure.

Defect Address Registers and Defect Marking Memory are required by Kim to record the detected faulty addresses or marking codes, i.e., the results of BIST. However, since the new **Claim 13** of the present invention dynamically updates the linked list according to the result of the BIST, Defect Address Registers and Defect Marking Memory are no longer required.

Similar to Kim, Chin performs BIST on all data rows of a packet buffer, **records the test results of all the data rows in a free link table,** and then generates the linked list according to the test results stored in the free link table (blocks 11-13). Specifically, similar to Kim's marking codes, Chin records the blocks of the free link table as "**fail**" or "**good**" according to the BIST results of all the data rows of the packet buffer, and then **reads all the blocks** of the free link table (i.e., reads all the fail/good marks in the free ink table) **when all the blocks are completed with recording** so as to initialize the blocks recorded as "good" in the free link table. That is, the BIST results of **all the data rows** of the packet buffer must be recorded

in the free link table **first** so that the linked list can be generated. Chin's approach is obviously different from the new **Claim 13** of the present invention. Therefore, the new **Claim 13** is patentably distinct from both Kim and Chin, and should be allowed.

Claims 14-18

Claims 14-18 are dependent upon claim 13, and should be allowable if claim 13 is found allowable.

Claim 19

In contrast to the new Claim 13, the new Claim 19 further limits both the contents of the linked list and the updating operations of the linked list. Accordingly, the new Claim 19 is also patentably distinct from both Kim and Chin, and should be allowed.

Claims 20-21

Claims 20-21 are dependent upon claim 19, and should be allowable if claim 19 is found allowable.

Claim 22

According to the same arguments under **Claim 13** and **Claim 19**, applicant believes that new Claim 22 has been placed in condition for allowance.

Since all newly entered claims of the present application are patentable over the cited prior art, the applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

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